

CLAIMS

1. Active load arrangement (Z) used to provide output DC
load to an object (TO) under AC test, which arrangement
5 (Z) comprises a voltage controlled transistor (MOSFET)
having a source (S), a gate (G) and a drain (D), which
drain (D) is associated with the gate (G) and connected
to an arrangement input (I2) associated with the object
(TO), and which source (S) is connected to an
10 arrangement output (O2) associated with the object
characterised by a feedback arrangement connected to the
source (S) and to the gate (G), which feedback
arrangement by varying frequency changes phase and
amplitude of the gate-to-source voltage to obtain low
15 impedance at low frequencies and high impedance at high
frequencies.
2. Active load arrangement according to claim 1, whereby
the feedback arrangement comprises a first feedback net
(FBN1) in which an inductance (L1) is connected between
20 the source (S) and the arrangement output (O2).
3. Active load arrangement (Z) according to claim 2,
whereby the feedback arrangement comprises a second
feedback net (FBN2) in which a first resistance (R1) is
connected between the gate (G) and the arrangement input
25 (I2), and a second resistance (R2) is connected between
the gate (G) and the source (S), and a capacitor (C1) is
connected between the gate (G) and the arrangement
output (O2).
4. Active load arrangement (Z) used to provide proper DC
30 output load to an object (TO) under AC test, which
arrangement (Z) comprises a voltage controlled
transistor (MOSFET) having a source (S), a gate (G) and
a drain (D), which drain is connected to an arrangement

input (I2) associated with an output (O1) of the object (TO), whereby a first resistance (R1) is connected between the gate (G) and the drain (D), characterised in that an inductance (L1) is connected between the source (S) and an arrangement output (O2) associated with an input (I1) of the object (TO), and that a capacitance (C1) is connected between the gate (G) and the arrangement output (O2).

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5. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to claim 4, whereby a second resistance (R2) is connected between the gate (G) and the source (S).
6. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to claim 4, whereby a second resistance (R2) is connected in parallel with the capacitance (C1).
7. Active load arrangement (Z) used to provide proper output load to an object (TO) under test according to any of claim 4-6, whereby a rectifier bridge is situated between the test object (TO) and the test arrangement (TA).
8. Active load arrangement (Z1) used to provide output load to an object (TO) under test, comprising an active load arrangement (Z) according to any of claim 1-3 and a second voltage controlled transistor (MOSFET2) comprising a second source (S2), a second gate (G2) and a second drain (D2), which second source (S2) is connected via the feedback arrangement to the source (S) and the gate (G) and via a fourth resistor (R4) to the second gate (G2), which gate (G2) is connected via a fifth resistance (R5) to the second drain (D2) and to an arrangement output (O3) associated with the test object

(T0) and which second gate (G2) is connected to the source (S) via a second capacitor (C2).